DR AMBEDKAR INSTITUTE OF TECHNOLOGY , BENGALURU-56

(An Autonomous Institution Affiliated to VTU, Belagavi, Accredited by NAAC with Grade "A" and Accredited by NBA)

Department of Electronics and Communication Engineering

LESSON PLANNING FOR THE ODD SEMESTER 2020-21

SEMESTER & SECTION	III		
SUBJECT CODE:	19EC31	SUBJECT :	Electronics Devices
REFERENCE DOC NO:		NO OF CREDITS :	03=3:3:0 (L - T – P)
		TOTAL NO OF HOURS:	39

Course Objectives

1	Understand the basics of semiconductor physics and electronic devices
2	Describe the mathematical models BJTs and FETs along with the constructional details
3	Understand the fabrication process of semiconductor devices and CMOS process integration
4	Understand the construction and working principles of MOSFET
5	Understand the construction and working principles of optoelectronic and high power devices and circuits

Pre-Requisitesfor this Course

1	Basics of Electronics
2	Basics of Physics
3	Mathematics-Differentiation and Integration
4	Frequencies and Time Domain Analysis

CLASS NO.	SYLLABUS			LESSON TEXT	Blooms Taxonomy Level.	CATEGORY			Teaching Methodology	Remarks
	UNIT	SUB UNIT	NO OF HRS			L	T	P		
				Overview of Syllabus: OBE, Course Objectives, Course Outcomes, Prerequisites and Applications of the subject.		√			**Plain Lecture**	
1	1	1	8	Semiconductor and p-n Junctions Bonding forces in sol	L1, L2	√			**Online class (Google Meet)**	

FACULTY

HOD

31-8-2020

2				Energy bands, Metals, Semiconductors and Insulators	L1, L2	√			Online class (Google Meet)	
3				Direct and Indirect semiconductors	L1, L2, L3	√			Online class (Google Meet)	
4				Electrons and Holes, Intrinsic and Extrinsic materials	L1, L2, L3	√			Online class (Google Meet)	
5				Conductivity and Mobility, Drift and Resistance	L3, L4	√			Online class (Google Meet)	
6				Effects of temperature and doping on mobility, Hall Effect	L3, L4	√			Online class (Google Meet)	
7				Forward and Reverse biased junctions- PN Junctions	L3, L4	√			Online class (Google Meet)	
11	2	1	8	Bipolar Junction Transistor Fundamentals of BJT operation	L3, L4	√			Online class (Google Meet)	
12				Amplification with BJTS, BJT Fabrication	L3, L4	√			Online class (Google Meet)	
13				The coupled Diode model (Ebers-Moll Model), Switching ope	L1, L2	√			Online class (Google Meet)	
14				Cutoff, saturation, switching cycle, specifications	L1, L2	√			Online class (Google Meet)	
15				Drift in the base region, Base narrowing	L3, L4	√			Online class (Google Meet)	
16				Avalanche breakdown, Base Resistance and Emitter crowding	L3, L4	√			Online class (Google Meet)	
17				Base Resistance and Emitter crowding	L1, L2	√			Online class (Google Meet)	
18				Capacitance and Charging times(hybrid-pi model)	L1, L2	√			Online class (Google Meet)	
19				Problems	L1, L2	√			Online class (Google Meet)	
43	3	1	7	Fabrication of p-n junctions-Thermal Oxidation	L3, L4	√			Online class (Google Meet)	
44				Diffusion, Rapid Thermal Processing	L1, L2	√			Online class (Google Meet)	

FACULTY

HOD
31-8-20

45				Ion implantation, chemical vapour deposition	L1, L2	√			Online class (Google Meet)	
46				photolithography, Etching	L1, L2	√			Online class (Google Meet)	
47				Metallization. Integrated Circuits: Background	L1, L2	√			Online class (Google Meet)	
48				Evolution of ICs: CMOS Process Integration	L3, L3	√			Online class (Google Meet)	
49				Evolution of ICs: CMOS Process Integration	L3, L4	√			Online class (Google Meet)	
50				Integration of Other Circuit Elements	L3, L4	√			Online class (Google Meet)	
22	4	1	8	Field Effect Transistors Basic p & n JFET Operation	L3, L4	√			Online class (Google Meet)	
23				MESFET operation	L3, L4	√			Online class (Google Meet)	
24				MOSFET	L1, L2	√			Online class (Google Meet)	
25				Two terminal MOS structure- Energy band diagram	L1, L2	√			Online class (Google Meet)	
26				Two terminal MOS structure- Energy band diagram	L1, L2	√			Online class (Google Meet)	
27				Depletion layer thickness	L1, L2	√			Online class (Google Meet)	
28				Work Function Difference	L1, L2	√			Online class (Google Meet)	
29				Work Function Difference	L1, L2	√			Online class (Google Meet)	
30				Flat band Voltage	L3, L4	√			Online class (Google Meet)	
31				Threshold Voltage, problems	L1, L2	√			Online class (Google Meet)	
32				Problems	L1, L2	√			Online class (Google Meet)	
33	5	1	8	Optoelectronic Devices Photodiodes intro	L1, L2	√			Online class (Google Meet)	
34				Current and Voltage in an Illuminated Junction	L1, L2	√			Online class (Google Meet)	
35				Current and Voltage in an Illuminated Junction	L1, L2	√			Online class (Google Meet)	

FACULTY

31-8-21

36				Solar Cells.	L1, L2	√			Online class (Google Meet)	
37				Photodetectors	L1, L2	√			Online class (Google Meet)	
38				Light Emitting Diode: Light Emitting materials	L1, L2	√			Online class (Google Meet)	
39				High Power devices: The P-N-P-N Diode	L3, L4	√			Online class (Google Meet)	
40				High Power devices: The P-N-P-N Diode	L3, L4	√			Online class (Google Meet)	
41				Insulated Gate Bipolar Transistor	L3, L4	√			Online class (Google Meet)	

Course outcomes: *After Successful Completion of the course the students should be able to*

CO1	Understand the principles of semiconductor Physics.
CO2	Understand the principles and characteristics of different types of semiconductor devices
CO3	Understand the fabrication process of semiconductor devices
CO4	Understand and utilize the mathematical models of semiconductor junctions and MOS transistors for circuits and systems.
CO5	Differentiate the semiconductor devices based on its usage and applications

This Course is the Prerequisite for

1	Linear Integrated Circuits
2	CMOS VLSI Design
3	Analog and Mixed Mode VLSI Design

FACULTY

HOD 31.8.2020

Blooms Taxonomy		
L1	REMEMBER	*Recall facts and basic concepts:* define, list, state
L2	UNDERSTAND	*Explain ideas or concepts:* classify, describe, discuss, explain, identify, recognize.
L3	APPLY	*Use information in new situations:* execute, implement, solve, demonstrate, sketch.
L4	ANALYZE	*Draw connection among ideas:* differentiate, organize, examine, test.
L5	EVALUATE	*Justify or decision:* argue, select.
L6	CREATE	*Produce new or original link:* design, assemble, construct, develop, formulate.

FACULTY

HOD

DR AMBEDKAR INSTITUTE OF TECHNOLOGY , BENGALURU-56

(An Autonomous Institution Affiliated to VTU, Belagavi, Accredited by NAAC with Grade "A" and Accredited by NBA)

Department of Electronics and Communication Engineering

LESSON PLANNING FOR THE EVEN SEMESTER 2021-22

SEMESTER & SECTION	VI A section (Batch 2019)	SUBJECT :	CMOS VLSI Design
SUBJECT CODE:	18EC61	NO OF CREDITS :	04=2:2:0 (L - T – P)
REFERENCE DOC NO:		TOTAL NO OF HOURS:	52

Course Objectives

1	Impart knowledge of MOS transistor theory and CMOS technologies
2	Learn the operation principles and analysis of inverter circuits, Understand basic circuit
3	Representation of different forms of diagrams like layout & stick diagram
4	Different CMOS logic structures
5	Analyze adder & multiplier circuits. Design Combinational, sequential and dynamic logic

Pre-Requisitesfor this Course

1	Basics of Electronics
2	Electronic Devices
3	Mathematics-Differentiation and Integration
4	Frequencies and Time Domain Analysis

CLASS NO.	SYLLABUS			LESSON TEXT	Blooms Taxonomy Level.	CATEGORY			Teaching Methodology	Remarks
	UNIT	SUB UNIT	NO OF HRS			L	T	P		
				Overview of Syllabus: OBE, Course Objectives, Course Outcomes, Prerequisites and Applications of the subject.		√			**Plain Lecture**	
1	1	1	10	Enhancement and Depletion mode operation MOS transistors (p & n type)	L1,L2	√			**Online/Chalk and Board, Asking Questions**	

FACULTY

HOD

2				MOS fabrication (p & n type)	L1,L2	√			Online/Chalk and Board, Asking Questions	
3				CMOS fabrication.	L1,L2	√			Online/Chalk and Board, Asking Questions	
4				MOS device design equations	L1,L2	√			Online/Chalk and Board, Asking Questions	
5				Second order effects of MOS	L1,L2	√			Online/Chalk and Board, Asking Questions	
6				Second order effects of MOS	L1,L2	√			Online/Chalk and Board, Asking Questions	
7				Static CMOS Inverter DC Characteristics	L1,L2	√			Online/Chalk and Board, Asking Questions	
8				Beta Ratio Effect, Noise Margin	L1,L2	√			Online/Chalk and Board, Asking Questions	
9				Pass Transistor, Transmission Gate, Tristate Inverter.	L1,L2	√			Online/Chalk and Board, Asking Questions	
10		2		Scaling of MOS Circuits: Scaling models and scaling fact	L1,L2	√			Online/Chalk and Board, Asking Questions	
11				Scaling factors for device parameters, Limitation of Scali	L1,L2	√			Online/Chalk and Board, Asking Questions	
12	2	1	9	Circuit Design Processes:	L1,L2	√			Online/Chalk and Board, Asking Questions	
13				MOS layers	L1,L2	√			Online/Chalk and Board, Asking Questions	

FACULTY

HOD

14				Stick diagrams.	L1,L2	√			Online/Chalk and Board, Asking Questions	
15				Design rules and layout.	L1,L2	√			Online/Chalk and Board, Asking Questions	
16				, lambda-based design rules.	L1,L2	√			Online/Chalk and Board, Asking Questions	
17		2		Basic Circuit Concepts:	L1,L2	√			Online/Chalk and Board, Asking Questions	
18				Sheet resistance, Area capacitances	L1,L2	√			Online/Chalk and Board, Asking Questions	
19				Capacitance calculations	L1,L2	√			Online/Chalk and Board, Asking Questions	
20				the delay unit	L1,L2	√			Online/Chalk and Board, Asking Questions	
21				Inverter delays	L1,L2	√			Online/Chalk and Board, Asking Questions	
22				driving capacitive loads	L1,L2	√			Online/Chalk and Board, Asking	
23	3	1	10	CMOS Logic Structures:	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
24				CMOS Complementary Logic	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
25				Pseudo-nMOS Logic	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
26				Dynamic CMOS Logic	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	

FACULTY

HOD

27				Clocked CMOS Logic,	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
28				Pass Transistor Logic	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
29				CMOS Domino Logic.	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
30				BiCMOS logic	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
31				Cascaded Voltage Switch Logic (CVSL)	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
32				Numericals	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
33	4	1	II	Datapath Subsystem I	L1,L2	√			Online/Chalk and Board, Asking	
34				Single bit addition	L1,L2	√			Online/Chalk and Board, Asking Questions	
35				carry generation & propagation	L1,L2	√			Online/Chalk and Board, Asking Questions	
36				PG Carry-Ripple Addition, Manchester carry chain adder	L1,L2	√			Online/Chalk and Board, Asking Questions	
37				carry skip adder, carry select, conditional sum adders	L1,L2	√			Online/Chalk and Board, Asking Questions	
38		2		DataPath Subsystems II	L1,L2	√			Online/Chalk and Board, Asking	
39				Unsigned Array Multiplication	L1,L2	√			Online/Chalk and Board, Asking Questions	

FACULTY

HOD

40				Complement Array Multiplication (Modified Baugh-Wooley two'	L1,L2	√			Online/Chalk and Board, Asking Questions	
41				Complement Array Multiplication (Modified Baugh-Wooley two's complement Multiplier)	L1,L2	√			Online/Chalk and Board, Asking Questions	
42				Booth encoding (Radix 4).	L1,L2	√			Online/Chalk and Board, Asking Questions	
43	5	1	12	Sequential MOS Logic Circuitry:	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
44				SR Latch Circuitry	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
45				SR Latch Circuitry	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
46				Clocked latch and Flip Flop Circuitry	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
47				Clocked latch and Flip Flop Circuitry	L1,L2,L3	√			Online/Chalk and Board, Asking	
48				Clocked latch and Flip Flop Circuitry	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
49				CMOS DLatch and Edge Triggered Flip-Flop	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
50				CMOS DLatch and Edge Triggered Flip-Flop	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
51				CMOS DLatch and Edge Triggered Flip-Flop	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	
52				Numericals	L1,L2,L3	√			Online/Chalk and Board, Asking Questions	

FACULTY

HOD